SUPPLEMENT TO WJ-8888 INSTRUCTION MANUAL

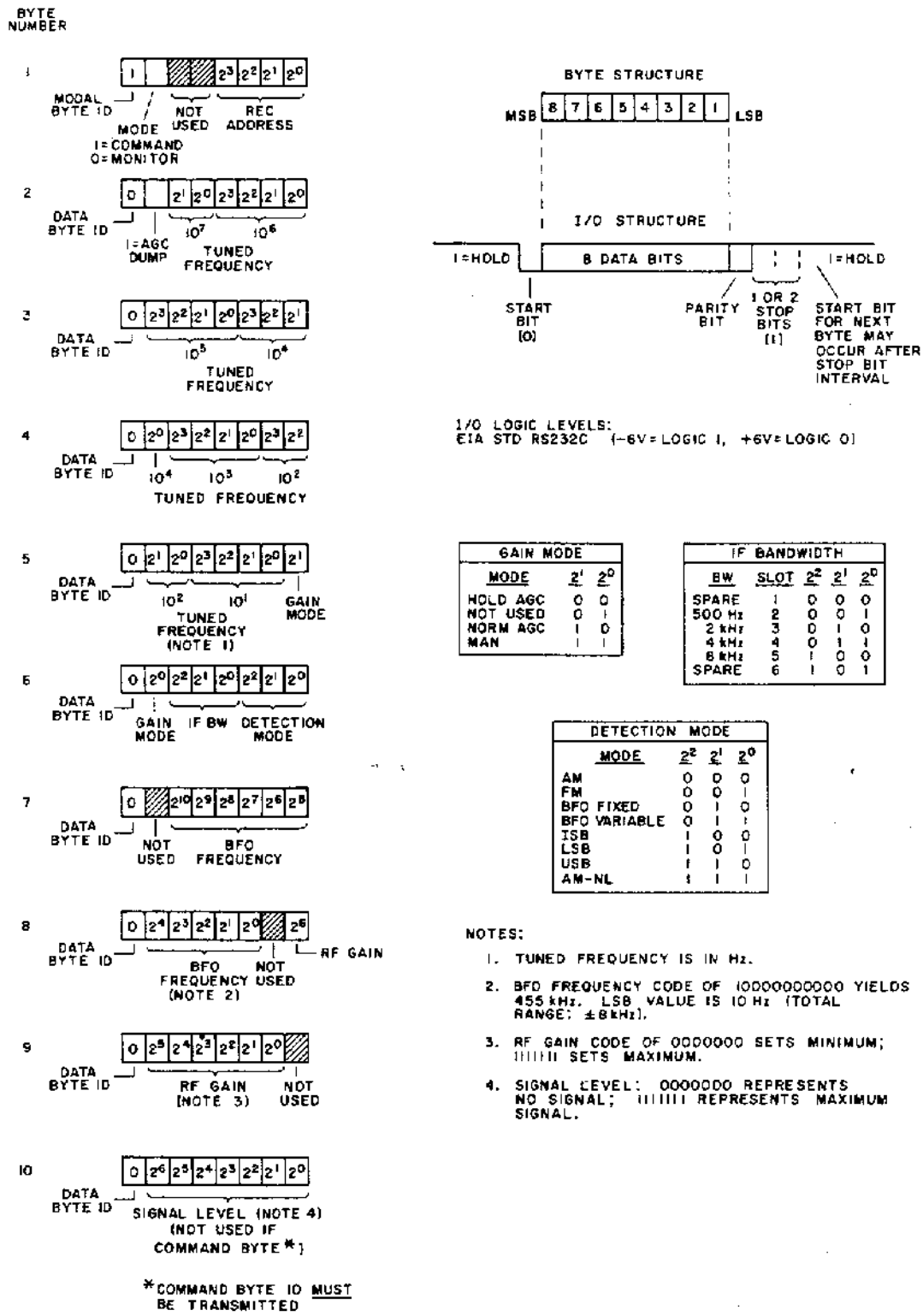
TYPE 791201 ASYNCHRONOUS I/O INTERFACE BOARD (A16)

I. INTRODUCTION. - The Asychronous I/O Board may be installed in the WJ-8888 as an option, in place of the standard synchronous I/O board, A16. The chosen I/O board is normally installed at the factory before the receiver is shipped, or the receiver may be converted in the field simply by interchanging boards. (NOTE: Earlier models may require additional chassis wiring for asynchronous I/O operation.)

Functionally, the asynchronous I/O differs from the synchronous I/O in that the data word is asynchronously shifted to or from shift registers on the I/O board instead of directly to or from an external computer. The data word in either shift register on the I/O board is previously obtained from the computer or later transmitted to the computer asynchronously. Asynchronous transmission/reception to or from the computer takes place by means of ten eleven-bit or twelve-bit bytes (see Figure 1). The first byte is a modal command byte, and each of the following nine bytes contain seven bits of the overall 64-bit data word. Start, stop, and parity bits are also included with each byte.

The I/O process begins with reception from the computer of a "modal byte" containing a modal byte identification bit and command/monitor select and receiver address bits. If the modal byte selects the command mode, the addressed receiver asynchronously accepts nine command data bytes, eliminates the start, stop, identification (ID), and parity bits from each byte, and assembles the remaining data in a shift register in serial format. This data word is sychronously clocked into the receiver register after all of the data has arrived. If, on the other hand, the modal byte selects the monitor mode, the addressed receiver returns the modal byte to the computer, then disassembles the stored serial data word seven bits at a time, and assembles each group of data bits into a byte containing ID, start, stop, and parity bits. Each of the nine data bytes is transmitted to the computer as it is generated.

II. STRAP SELECTABLE OPTIONS. - Strap selectable options are listed in Table 1. Baud rate, parity mode, stop bit, and receiver ID selections are with reference to the modal and data bytes shown in Figure 1, and require no further explanation except to mention that these parameters must be selected for compatibility between computer and receiver or between master and slave units. If master/slave operation is selected, the receiver with no jumper between E28 and E29 functions as a master to another receiver of the same address. That is, without requiring reception of a modal byte from a computer, the master receiver continually produces ten-byte monitor output groups, which may be used to control another receiver if applied to the command input of that receiver. The slave receiver control settings will (if operated in the remote mode) exactly follow the master receiver control settings (with exception of parameters not remotely controllable).



GAIN MODE		
MODE	2^1	2^0
HOLD AGC	0	0
NOT USED	0	1
NORM AGC	1	0
MAN	1	1

IF BANDWIDTH				
BW	SLOT	2^2	2^1	2^0
SPARE	1	0	0	0
500 Hz	2	0	0	1
2 kHz	3	0	1	0
4 kHz	4	0	1	1
8 kHz	5	1	0	0
SPARE	6	1	0	1

DETECTION MODE			
MODE	2^2	2^1	2^0
AM	0	0	0
FM	0	0	1
BFO FIXED	0	1	0
BFO VARIABLE	0	1	1
ISB	1	0	0
LSB	1	0	1
USB	1	1	0
AM-NL	1	1	1

NOTES:

1. TUNED FREQUENCY IS IN Hz.
2. BFO FREQUENCY CODE OF 1000000000 YIELDS 455 kHz. LSB VALUE IS 10 Hz (TOTAL RANGE: ±8 kHz).
3. RF GAIN CODE OF 0000000 SETS MINIMUM; 1111111 SETS MAXIMUM.
4. SIGNAL LEVEL: 0000000 REPRESENTS NO SIGNAL; 1111111 REPRESENTS MAXIMUM SIGNAL.

Figure 1. Asynchronous I/O Data Word Diagram

Table 1. Strap Selectable Options On Asynchronous I/O Interface

1. Baud Rate

Jumper E27 to:	For Baud Rate Of:
E26	75
E25	150
E24	300
E23	600
E22	1200
E21	2400
E20	4800
E19	9600

2. Parity Mode

A. No jumper between E3 and E4, no parity.
B. No jumper between E1 and E2 and jumper between E3 and E4, even parity.
C. Jumper between E1, E2 and E3, E4, odd parity.

3. Stop Bit

Jumper between E5 and E6 - single stop bit; no jumper between E5 and E6 - two stop bits.

4. Receiver ID

The Receiver ID is coded according to following table.

RCVR ID	E11-E12	E13-E14	E15-E16	E17-E18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

A '0' represents a short between the electrical lugs and a '1' represents an open.

5. Normal-Master/Slave Operation

Jumper between E28 and E29 - normal operation; no jumper - Master unit for Master/ Slave operation.

III. INTERFACE CONNECTIONS. - The main chassis schematic in the WJ-8888 manual shows the DIGITAL CONTROL connector pin designations for the asynchronous I/O board as well as for the synchronous I/O board. With the asynchronous I/O board installed, up to sixteen differently addressed receivers may be interfaced with the computer by dual loop-through ("daisy-chain") connections to common command and monitor lines. Typical connections are shown in Figure 2. Interface connector types are listed in Table 2-1 of the instruction manual (Bendix JTG06RT12-22P-SR), and are supplied as part of the original receiver shipment. The command data input and output lines of the receivers, when connected in a daisy chain configuration, permit the modal byte and following nine bytes (if command mode) to be applied to all sixteen receivers in common. Only the receiver which responds to the address will digest the data. If, on the other hand, the modal byte commands the monitor mode, the addressed receiver, instead of receiving data bytes, will return the modal byte and nine monitor data bytes to the computer via the daisy chain. (Transmitter gating circuits in receivers not addressed but situated closer to the computer through-route the monitor bytes.) Computer interfacing is by means of EIA standard RS232C logic (-6 V for logic 1, +6 V for logic 0, tri-state RZ format).

IV. CIRCUIT DESCRIPTION. - Before proceeding with a description of the dynamics of the overall circuit, it is appropriate to identify the abbreviations used and to describe some of the specialized circuits on the I/O board. For abbreviations, refer to Table 2. Specialized circuits are covered in the following paragraphs.

Asynchronous Receiver/Transmitter and Shift Registers. - The heart of the I/O board is U10, which is a programmable asynchronous receiver transmitter module. The receiver section of U10 verifies proper code transmission of each byte serially received from the remote control unit, by checking parity and receipt of a proper stop bit, and provides the data bits on parallel output lines. The transmitter section adds start, stop, and parity bits to the data presented on parallel input lines, and serially shifts each byte thus generated to the remote control unit.

For transmission, the 64-bit data word is first synchronously shifted from the digital control section of the receiver into 64-bit shift register U8. The data word is then shifted seven bits at a time into holding register U9. Each set of seven bits is parallel loaded into U10 (pins 26 through 32) for transmission as part of a serial byte to which start, stop, and parity bits are added. Pin 25 is the transmitter output.

For reception, the receiver section of U10 provides data received (pin 19) and error flag outputs (pins 13, 14, 15) for each byte received on pin 20, and provides data on parallel output pins 5 through 12 for loading into holding register U25. Each set of seven data bits loaded into U25 is immediately shifted into 64-bit register U26, so that the next set of data bits may be loaded into U25. After all of the data is received, the 64-bit data word in U26 is synchronously transferred to the digital control section of the receiver.

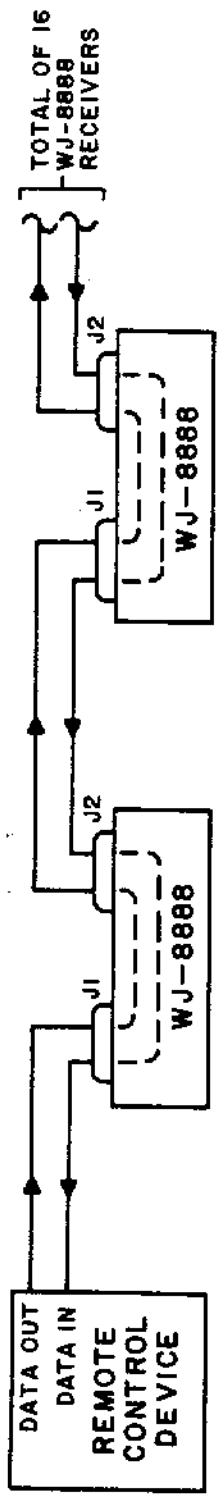


Figure 2. Typical Interface Connections

Table 2. Abbreviations

Abbreviation	Meaning
RI	Receiver Input
THRL	Transmitter Holding Register Load
RRD	Receiver Register Disconnect
SFD	Static Flags Disconnect
TRE	Transmitter Register Empty
EPE	Even Parity Enable
PI	Parity Inhibit
SBS	Stop Bit Select
DRR	Data Received Reset
WLS	Word Length Select
CRL	Control Register Load
RR	Receiver Register Parallel Output
DR	Data Received
MR	Master Reset
OE	Overrun Error
FE	Framing Error
PE	Parity Error
TRO	Transmitter Register Output
TRC	Transmitter Register Clock
RRC	Receiver Register Clock
TR	Transmitter Register Parallel Input
MON	Monitor Line (U30B pin 6)
COM	Command Line (U31D pin 11)
CCI	Command Counter Increment
MON RST	Monitor Reset
INIT	Initialization (Upon Power On)
CC	Command Counter (U17A)
MC	Monitor Counter (U17B)
MCI	Monitor Counter Increment
EOC	End of Cycle (Digital Control Section) (Pulse)
M	Monitor Mode
MCO	Monitor Counter (U17B) Zero
CCO	Command Counter (U17A) Zero
SS	Self Sync
MUX (OS)	Multiplexer One-Shot
ID	Identification

Parallel loading of the address code into U9 and other details concerning operation of U8, U9, U10, U25, and U26 are covered in the description of the overall circuit operation given below.

Clock Circuit. - The clock circuit consists of the 3.9936 MHz oscillator comprising Y1 and U39 B and F, buffer U39C, divide-by-thirteen divider comprising U1 and U42A, and binary counter/divider U2. The oscillator is a straightforward crystal controlled circuit. U1 is a synchronous 4-bit binary counter connected such that its carry output is applied back to its parallel entry command input. On the first clock pulse (oscillator output pulse) after full count, therefore, the counter presets to a count of 3, as determined by the fixed levels applied to the parallel data inputs (pins 3 through 6). This effectively subtracts 3 from the total numerical count capacity of 16, so that division by 13 is accomplished. (The output of U1 is 307.200 kHz.) The frequency is further divided by binary divider U2. The successive stages of U2 divide by factors of two. The user may select the desired baud rate by connecting jumper JW3 to the appropriate divider output. The bit frequency at each output of U2 is sixteen times the baud rate indicated. The clock circuit output is used to clock the shift registers in U10 and also clocks the self sync divider circuit (U23A, U41).

7-Shift Clock Generators. - Two identical seven-shift clock generators are utilized for shifting data in groups of seven bits to and from holding registers U9 and U25. Certain reset and gating outputs are also provided by these circuits. The seven-shift clock generator associated with the transmitter section is composed of U5B, U15B, U14D, U13, and U15A; the seven-shift clock generator associated with the receiver section is composed of U20A, U20B, U43C, U21, and U23B. 200 kHz IC clock U19 is common to both circuits. Since both seven-shift clock generator circuits are identical, the one associated with the receiver section is here explained as representative of both.

U20A, U20B, and U23B are D-type flip-flop MV's, and U21 is a decade counter with decimal decoder. Pin 6 of U21 goes high on the seventh count after zero reset. Assume, initially, that the seventh count has occurred and pin 6 of U21 is high, and assume that no further initiating trigger is received on pin 11 of U20B. The mode of operation of U20A, to be explained shortly, is such that logic low must appear on the data input (pin 5) in order that the circuit produce a trigger pulse. Therefore, while U21 holds at count seven the Q output of U20A holds at logic high and the $\overline{Q}$ output holds at logic low. Logic low applied by U20A to the reset input of U20B does not reset U20B, and in the absence of a trigger pulse the logic high on the data input (pin 9) is not clocked through. Therefore, the Q output of U20B remains at a logic low which was set up by a reset input provided by U20A during the previous counting cycle. The logic low output of U20B does not reset U21 and therefore U21 holds at the count of seven. (The logic low also permits U25 to remain in the serial mode. Note that when in the hold condition, the logic-high Q output of U20A enables U22D, so that Clock 2 from the digital control section may shift data from U25 and U26.)

Upon receipt of a logic high transition on the clock input (pin 11) of U20B, the logic high on the data input (pin 9) is transferred to the Q output (pin 13), which resets U21 (and also causes shift register U25 to change to the parallel entry mode). The first clock pulse from U19 transfers the logic low from the data input (pin 5) of U20A to the Q output. The logic high from the complementary $\overline{Q}$ output resets U20B to a logic low output, thus removing the reset applied to U21 (and returning U25 to the serial mode). The logic-low Q output of U20A and the low on pin 9 of U43C which occurs on the trailing edge of the U19 lock pulse, produce a logic high at the output of U43C which is applied to the set input (pin 6) of U20A. This set input returns the Q output to logic high, which transition clocks U21 and provides a clock output to U25 and U26 via U22D and U24. U20A continues to provide clock pulses until U21 again reaches the count of seven, at which time the circuit returns to its previously described hold condition. The logic high transition on the count of seven clocks U23B, so that the Q output of U23B goes high and the $\overline{Q}$ output goes low. The next clock pulse from U19 resets U23B to its previous condition, which remains until the next seventh count occurs.

Address Decoder. - Exclusive OR gates U27A through D and NOR gate U28B decode the address on the first modal byte received. Jumpers should be connected as appropriate to terminals E11 through E18 to select the desired address code for this receiver (decimal equivalent 0 through 16), as listed in Table 1. When this receiver is addressed the output of U28B goes high. Note that the address code is applied to the transmitter holding register parallel inputs, for return to the remote computer as part of the first modal byte when in the monitor operating mode.

One-Shot Multivibrators. - One-shot MV's are employed on this board where it is desired to convert logic level shifts to short trigger pulses. Each MV is composed of two buffer drivers and an RC charging circuit. U6E, U12A, R4, and C20 is one MV, U24A and B, R6, and C23 is another MV, and U36D, U24F, R7, and C22 is a third MV. Although they differ slightly in input, output, or charging levels, they all function on the same basic principle. That is, an input level change causes the output level to change for the duration of the charging or discharging of the capacitor through the corresponding resistor. When the capacitor is sufficiently charged or discharged, because the output buffer is a two-state device, the output quickly returns to the original level. Return of the input to the orhginal level does not produce another output pulse, and the capacitor charges or discharges to the quiescent level.

TTL/RS232C Level Converters and Comparator Interfacing. - Interfacing with the computer is by way of EIA standard RS232C logic levels (-6 V for logic 1, +6 V for logic 0). U4A and U4B are RS232C-to-TTL logic converters, and U3A and U3B are TTL-to-RS232C logic converters. The command input is converted to TTL by U4A and applied to the receiver input of U10, and is also returned to the interface connector via logic converter U3A. By a similar arrangement, the transmitter output of U10 is applied to a gating circuit (U34A, B, D) which selects either the

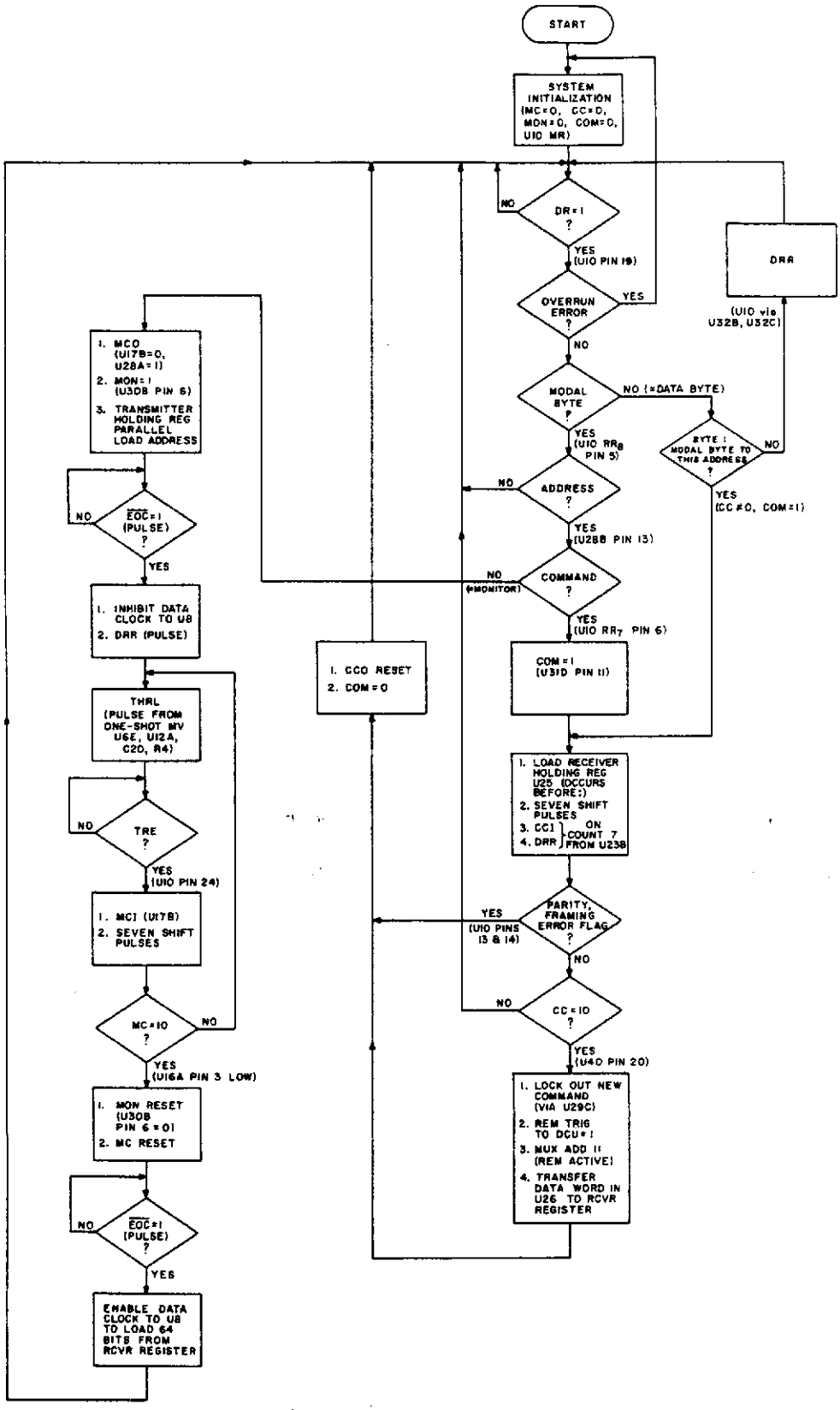


Figure 3. Flow Chart, Asynchronous I/O

U10 transmitter output or the output of logic converter U4B, depending on the operating mode of the I/O module, for application to the computer via output logic converter U3B. These input/output configurations permit up to sixteen differently addressed receivers to be interfaced with the computer by dual loop-through ("daisy-chain") connections to common command and monitor lines. The command data input and output lines of the receivers, when connected in a daisy chain configuration, permit the modal byte and following nine data bytes (if command mode) to be applied to all sixteen receivers in common. Only the receiver which responds to the address will digest the data. If the modal byte commands the monitor mode, on the other hand, the addressed receiver, instead of receiving data bytes, will return the modal byte and nine monitor data bytes via the monitor daisy chain line. The transmitter gating circuits (U34A, B, D) of receivers not addressed but situated closer to the computer, through-route these modal and monitor data bytes.

Overall Circuit Operation. - Reference to the Flow Chart, Figure 3 will be of help in understanding the following description of the dynamics of the asynchronous I/O module. Note that the flow chart branches into command and monitor paths. The following description first follows the command path, then the monitor path.

(1) Power-On Initialization. - Upon power turn-on or return from power failure, the output of U42C is initially high. C26 charging through R24 causes the output of U42C to go low after a short delay. The initial logic high output of U42C, applied to the master reset input of U10 via U14C and U35E, resets all of the circuitry in U10. The corresponding initial logic low output of U14C presets monitor latch U30A-B so that pin 6 of U30B is low, presets command latch U31D-U30C so that pin 11 of U31D is low, forces the output of U33A to go high and reset command counter U17A to zero, and resets monitor counter U17B to zero via U18C. When C26 charges sufficiently, the output of U42C goes low, thus removing the preset logic levels and permitting the various circuits to operate normally.

(2) The receiver section of U10 is now receptive to data from the computer (applied to the RI input, pin 20). When U10 senses that it has received a byte, the Data Received (DR) output, pin 19, goes high. In addition, if the data received is a modal byte, as indicated by bit 8 (see Data Word Diagram, Figure 1), the bit 8 (pin 5) output of U10 goes high. (If not a modal byte, then must be command data byte. See (7) below. Also, if the address decoder circuit (U27 A-D, U28B) senses that this receiver is addressed by bits 1 through 4 of the modal byte, the output of U28B goes high. These three high levels, occurring simultaneously, enable NAND gate U29B, causing the output of U35A to go high. Note that if an overrun error exists, the OE output of U10 produces an initiate logic low from U14C which resets all of the circuitry as described in (1) above, thus invalidating all data received or transmitted to date.

(3) If step (2) is satisfied, and in addition bit 7 of the modal byte, obtained from pin 6 (RR7) of U10, is high, indicating a command cycle request, the output of U29C goes low, presetting command latch U31C-U31D (U31D pin 11 high). If,

on the other hand, bit 7 is low, the circuit will instead go through a monitor cycle, as described starting with step (10) below.

(4) Because of the initial reset of the command counters pin 11 of converter U40 is high, causing a high output from U37C which enables U37B. Therefore, the logic low output transition from U29C, which occurs on reception of a command modal byte as described in (3) above, causes the output of U37B to go high, thus triggering the receiver seven-shift clock generator. The seven-shift clock generator first causes U25 to parallel-load the modal byte, then generates seven clock pulses which serially shifts this data into 64-bit register U26 (see circuit description above). Note that the total bit count of the ten bytes which are to be received is 70, and U26 can hold only 64 bits. This first byte will eventiclly be discarded by being clocked out of U26 upon clocking in of the tenth byte (9th data byte).

(5) U23B is clocked on count seven of the seven-shift clock generator. The resulting $\overline{Q}$ output transition of U23B is applied to command counter U17A, via NAND gate U38A, thus incrementing the counter. The Q output transition of U23B, applied to the DRR input of U10 via U32C, resets the receiver section of U10 so that a new byte may be received from the computer.

(6) If U10 senses a parity or framing error the output of U35C will go low and reset the command counter and the command latch, thus invalidating the entire set of data received to date, and a new set of data must be transmitted by the computer.

(7) Up to this point we have described reception of a command modal byte. Therefore, the command counter holds the count of one, causing both outputs of converter U40 to be low. These logic lows and the logic high command line render the circuit receptive to a data byte from the computer. The data byte lacks address and command bits, but the logic-low identification bit (RR8, pin 5 of U10) and the DR output of U10 cause the output of U43 to go high, which transition is routed to the seven-shift clock generator clock input via U37C and U37B. The seven-shift clock generator parallel loads the data into U25, shifts this data into U26, and on the count of 7 clocks U23B so that command counter U17A is incremented and U10 receives a reset pulse on pin 18 as before. If the command counter is at zero, however, this is an indication that the byte should be a modal byte, and reception of a data byte will reset the receiver section circuits in U10 (DRR via U23B and U32C) but a trigger pulse will not be provided to the seven-shift clock generator.

(8) As with the modal byte, a parity or framing error flag will reset the circuit.

(9) The circuit continues receiving and loading data bytes from the computer until the command counter reaches the count of ten. The resulting logic high from pin 20 of binary-to-decimal converter U40 is inverted by U24C to disable

U29C, thus locking out receipt of a new command modal byte. The logic high from U40 pin 20 also provides a remote trigger to the digital control section of the receiver, resulting in the generation of a remote-active mux address code (11) which is returned to this board. The output of U24E therefore goes high, permitting NAND gate U22A to pass C2 pulses provided by the digital control section. The complete 64-bit data word stored in shift register U26 is therefore clocked into the receiver register of the digital control section during period 1 of the receiver control cycle. In addition, the pulse generated by one-shot MV U24F, U36D, C22, and R7 and passed by U31B and U35C resets the command counter and command latch, thus preparing the circuit for reception of the next modal byte from the computer.

(10) Refer back to steps (1), (2), and (3), and assume that bit 7 of the modal byte is low, indicating a monitor command. The corresponding logic-low RR7 output (pin 6) of U10 disables U29C and is inverted by U35B. The logic high from U35B and an address decision logic high from U35A cause the output of NOR gateU31C to go low. This logic low resets monitor counter U17B to zero and causes transmitter holding register U9 to parallel-load an address code (determined by jumpers E11 through E18) and other bits (including a bit-8 high - since monitor counter U17B is at zero) which render the byte identical to the received monitor modal byte. The parallel-loaded data appears immediately at the outputs of U9. The monitor mode logic low from U31C also sets monitor latch U30A-U30B such that the monitor line (U30B pin 6) is high. Since the monitor line is applied to the data input of U5A, the next EOC pulse causes the Q output of U5A to go high, inhibiting the data clock to U8. The complementary $\overline{Q}$ output logic low transition causes the one-shot MV comprising U6E, U12A, C20, and R4 to produce a positive pulse. The resultant low-going pulse from U32A causes the monitor modal byte appearing at the parallel outputs of U9 to be loaded into the transmitter holding register of U10, from which it is clocked out to the remote computer via U34D (refer to the computer interfacing circuit description above.) The pulse from the one-shot MV is also applied to the data received reset (DRR) input of U10 via U32C, thus removing the modal byte from the receiver register outputs, which in turn causes the monitor mode line (U31C pin 10) to go high and U9 to revert to the serial operating mode.

(11) Note that prior to reception of the monitor modal byte, logic low applied to the data input (pin 5) of U5A produces a logic-high $\overline{Q}$ output from U5A when U5A receives an EOC pulse from the digital control section of the receiver. NAND gate U7A is therefore able to pass data clock pulses from the digital control section to the clock input of shift register U8 via NAND gate U29A. Therefore, we assume initially that at the beginning of a monitor mode, the entire 64-bit data word from the digital control sections's receiver register is stored in shift register U8.

(12) When the monitor modal byte is completely clocked out of the transmitter register of U10, U10 produces a Transmitter Register Empty (TRE) logic high, which increments the monitor counter and clocks the transmitter seven-shift

clock generator. Seven shift clock pulses from U5B pin 12 are applied to U8, via U7B and U29A, and to the clock input of U9. Thus seven data bits are transferred from U8 to U9.

(13) On count seven U15A produces a pulse which is applied via U32A to the THRL input of U10. The transmitter holding register in U10 therefore parallel-loads the seven bits of the data word which were shifted into U9. Also, since monitor counter U17B is no longer at zero, the output of U28A is low. Therefore U10 loads a logic-low bit 8, which identifies the byte as a data byte.

(14) U10 adds start, stop, and parity bits, and shifts the entire data byte to the remote computer via the TRO output of U10, NAND gates U34D and U34A, and logic converter U3B.

(15) As long as U17 has not reached the count of 10, no monitor reset pulse is produced. Therefore when the transmitter register is empty U17B and the seven-shift clock generator are clocked again, so that seven more data bits are transferred from U8 to U9 to begin the formation of a new data byte for transfer to the remote computer. Data bytes will continue to be produced until U17B reaches the couunt of 10, as detected by NAND gate U38C. When this occurs U16A becomes enabled so that as soon as the last byte is transferred to the computer, the TRE logic high causes a logic-low monitor reset output from U16A. This monitor reset level resets monitor counter U17B and monitor latch U30A-U30B.

(16) With the monitor line now low, the next EOC pulse from the remote control unit changes the states of the outputs of U5A so that NAND gate U1B is disabled and NAND gate U7A is enabled. This permits data clock pulses to transfer a new 64-bit data word from the receiver register in the remote control unit into U8, thus performing the final step in readying the I/O circuit for reception of a new command or monitor modal byte.

TYPE 791201 ASYNCHRONOUS I/O REF DESIG PREFIX A16

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	CAPACITOR, ELECTROLYTIC, TANTALUM: 47 μF, 10%, 20 V	5	CS13BE476K	81349	56289
C2	CAPACITOR, CERAMIC, DISC: 0.1 μF, 20%, 100 V	15	8131M100-651-104M	72982	
C3 Thru C10	Same as C2				
C11	Same as C1				
C12	Same as C2				
C13	Same as C1				
C14	Same as C2				
C15	Same as C1				
C16	Same as C2				
C17	Same as C1				
C18	Same as C2				
C19	CAPACITOR, MICA, DIPPED: 750 pF, 5%, 300 V	1	DM15-751J	72136	
C20	CAPACITOR, CERAMIC, DISC: 1000 pF, GMV, 500 V	3	SM (1000 pF, F)	91418	
C21	CAPACITOR, MICA, DIPPED: 20 pF, 5%, 500 V	1	CM05ED200J03	81349	72136
C22	Same as C20				
C23	Same as C20				
C24	Same as C2				
C25	Same as C2				
C26	CAPACITOR, ELECTROLYTIC, TANTALUM: 1 μF, 10%, 35 V	1	CS13BF105K	81349	56289
R1	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/4W	2	RCR07G101JS	81349	01121
R2	Same as R1				
R3	RESISTOR, VARIABLE, FILM: 5 kΩ, 10%, 1/2W	1	62PR5K	73138	
R4	RESISTOR, FIXED, COMPOSITION: 15 kΩ, 5%, 1/4W	3	RCR07G153JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 330 Ω, 5%, 1/4W	2	RCR07G331JS	81349	01121
R6	Same as R4				
R7	Same as R4				
R8	RESISTOR, FIXED, COMPOSITION: 3.3 kΩ, 5%, 1/4W	13	RCR07G332JS	81349	01121
R9 Thru R11	Same as R8				
R12	RESISTOR, FIXED, COMPOSITION: 10 kΩ, 5%, 1/4W	1	RCR07G103JS	81349	01121
R13 Thru R18	Same as R8				
R19	NOT USED				

REF DESIG PREFIX A16

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R20	Same as R8				
R21	Same as R8				
R22	Same as R5				
R23	RESISTOR, FIXED, COMPOSITION: 200 Ω, 5%, 1/4W	1	RCR07G201JS	81349	01121
R24	RESISTOR, FIXED, COMPOSITION: 5.1 kΩ, 5%, 1/4W	1	RCR07G512JS	81349	01121
R25	Same as R8				
U1	INTEGRATED CIRCUIT	1	SN74161N	01295	
U2	INTEGRATED CIRCUIT	2	CD4040AE	02735	
U3	INTEGRATED CIRCUIT	1	SN75150N	01295	
U4	INTEGRATED CIRCUIT	1	SN75152N	01295	
U5	INTEGRATED CIRCUIT	4	CD4013AE	02735	
U6	INTEGRATED CIRCUIT	5	CD4049AE	02735	
U7	INTEGRATED CIRCUIT	6	CD4011AE	02735	
U8	INTEGRATED CIRCUIT	2	CD4031AE	02735	
U9	INTEGRATED CIRCUIT	1	CD4034AD	02735	
U10	INTEGRATED CIRCUIT	1	TR1602A	52840	
U11	INTEGRATED CIRCUIT	3	CD4050AE	02735	
U12	Same as U11				
U13	INTEGRATED CIRCUIT	2	CD4017AE	02735	
U14	INTEGRATED CIRCUIT	1	CD4001AE	02735	
U15	Same as U5				
U16	Same as U7				
U17	INTEGRATED CIRCUIT	1	MC14520P2	04713	
U18	INTEGRATED CIRCUIT	4	CD4023AE	02735	
U19	INTEGRATED CIRCUIT	1	MC4024P	04713	
U20	Same as U5				
U21	Same as U13				
U22	Same as U7				
U23	Same as U5				
U24	Same as U6				
U25	INTEGRATED CIRCUIT	1	CD4021AE	02735	
U26	Same as U8				
U27	INTEGRATED CIRCUIT	1	CD4030AE	02735	
U28	INTEGRATED CIRCUIT	1	CD4002AE	02735	
U29	Same as U18				
U30	Same as U18				

REF DESIG PREFIX A16

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U31	Same as U7				
U32	INTEGRATED CIRCUIT	1	CD4025AE	02735	
U33	INTEGRATED CIRCUIT	1	CD4012AE	02735	
U34	Same as U7				
U35	Same as U6				
U36	Same as U11				
U37	Same as U18				
U38	Same as U7				
U39	INTEGRATED CIRCUIT	1	867404	14632	
U40	INTEGRATED CIRCUIT	1	CD4514BD	02735	
U41	Same as U2				
U42	Same as U6				
U43	INTEGRATED CIRCUIT	1	CD4001AE	02735	
U44	Same as U6				
VR1	VOLTAGE REGULATOR	2	1N759A	80131	
VR2	Same as VR1				
Y1	CRYSTAL, QUARTZ	1	CR66/U (3.9936 MHz)	80058	74306

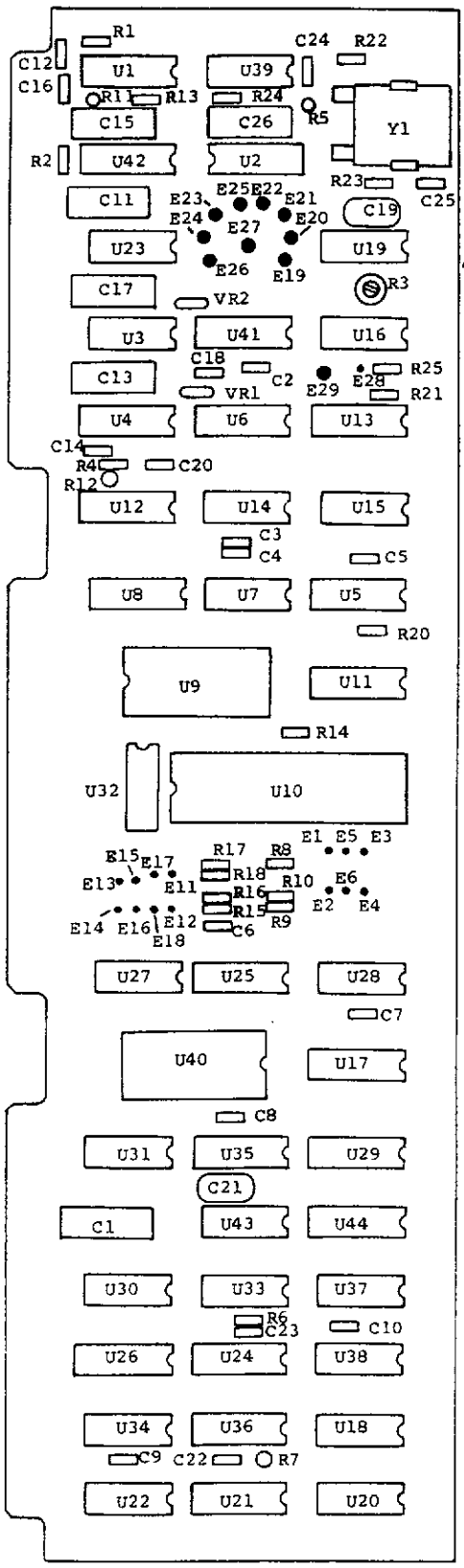
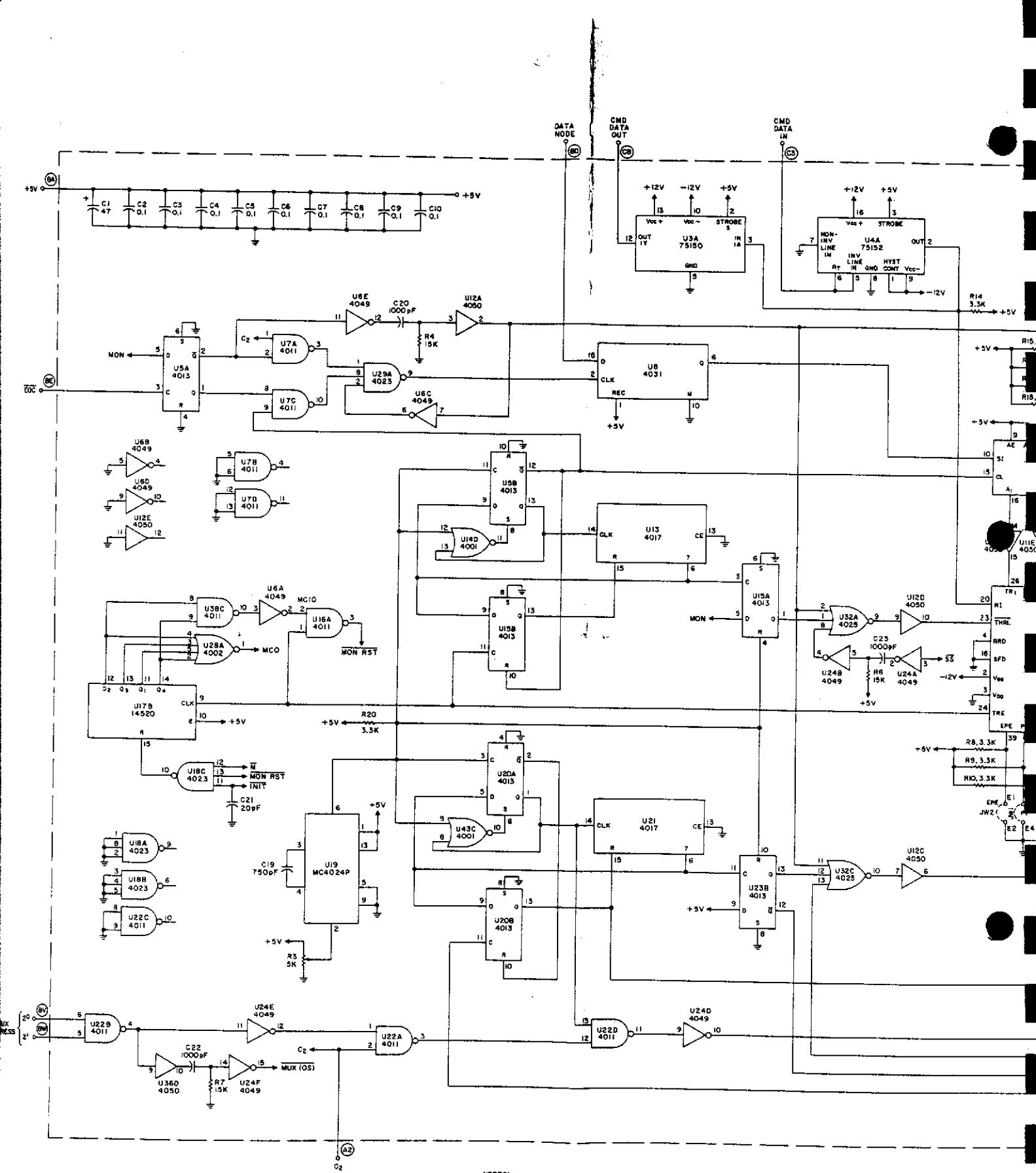


Figure 4. Type 791201 Asynchronous I/O, Component Locations



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. ENCIRCLED LETTERS (NUMBERS) ARE MODULE PIN CONNECTIONS.
3. Vcc, Vee, AND GND CONNECTIONS, PIN ARRANGEMENT, AND SPARE CIRCUITS OF IC'S ARE GIVEN IN TABLE I.

IC TYPE	4001	4002	4011
REF DESIGS	U14 U43	U28	U22, U7, U16, U34, U38
PIN ARR/DETAIL	A	A	A
Vcc (+5V)	14	14	14
GND	7	7	7
Vee (-V)			
SPARES	U14A U43B,D		U22C, U7B,D U16A, U34C, U38B

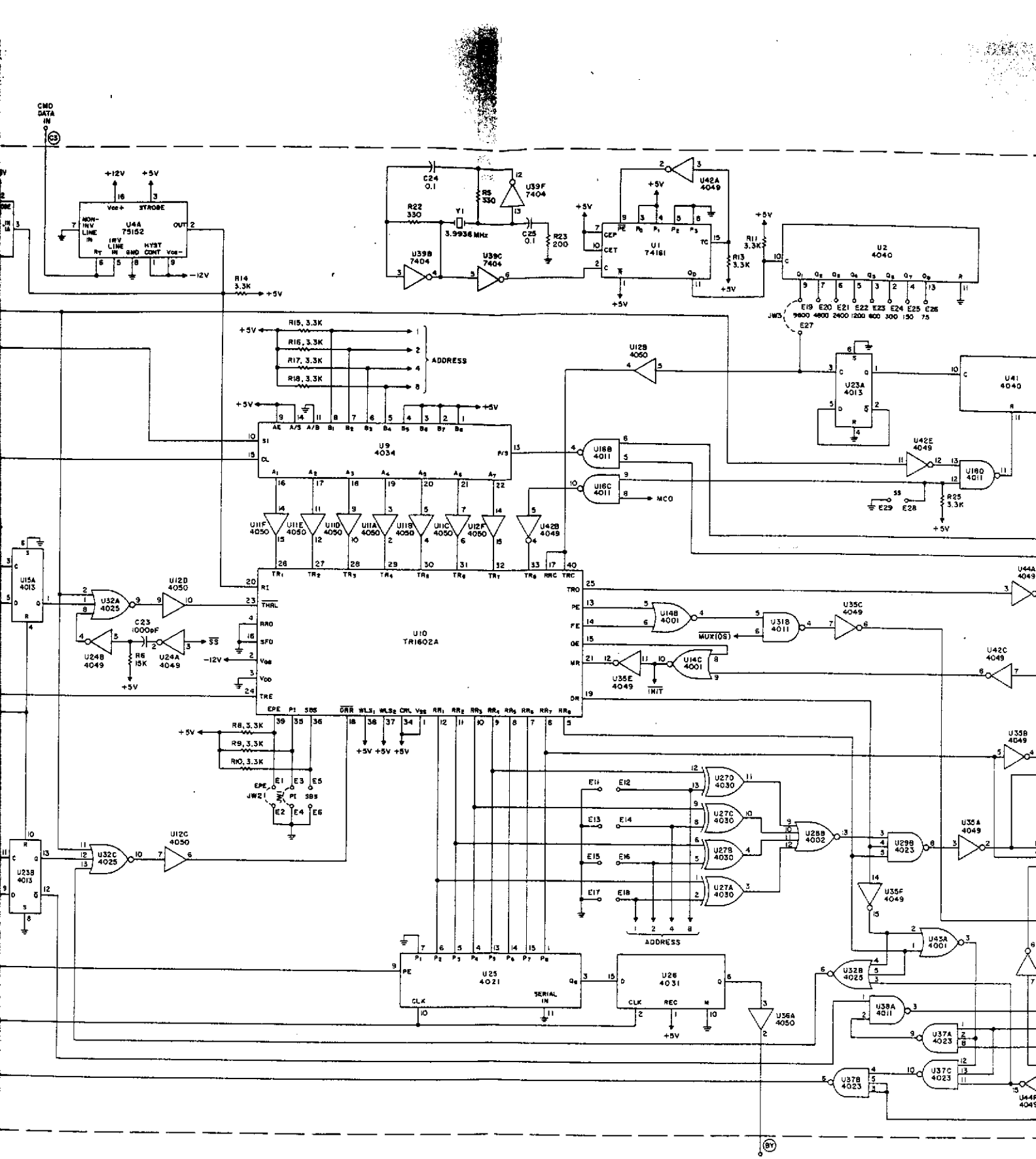
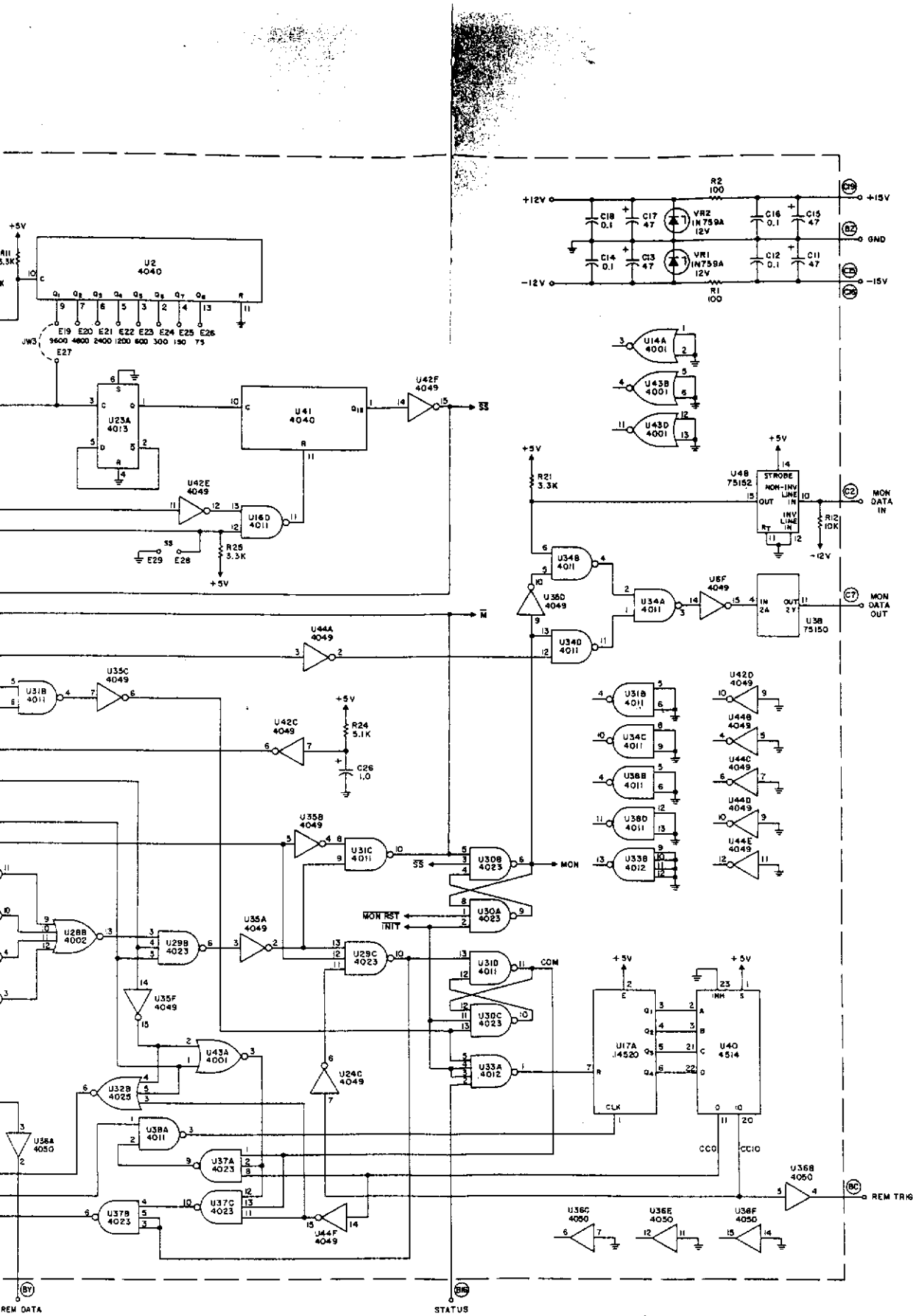


TABLE I

IC TYPE	4001	4002	4011	4012	4013	4017	4021	4023	4025	4030	4031	4034	4040	4049	4050	4514	7404	14520	74161	75150	75152	TR1602A	MC4024P
REF DESIGS	U14 U43	U28	U22, U7, U16, U31 U34, U38	U33	U5, U15 U20, U23	U13 U21	U25	U18, U29 U30, U37	U32	U27	U8 U26	U9	U2 U41	U6, U35, U42, U44 U24	U11, U12 U36	U40	U39	U17	U1	U3	U4	U10	U19
PIN ARR/DETAIL	A	A	A	A	A	B	B	A	A	A	B	C	B	B	B	C	A	B	B	A	B	D	A
Vcc (+5V)	14	14	14	14	14	16	16	14	14	14	16	24	16	1	1	24	14	16	16	(+12V) 13	(+12V) 14	1	14
GND	7	7	7	7	7	8	8	7	7	7	8	12	8	8	8	12	7	8	8	5	8	3	7
Vee (−V)																				(−12V) 10		(−12V) 2	
SPARES	U14A U43B,D		U22C, U7B,D U31A, U34C, U38B,D	U33B				U18A,B						U6B,D & U42D U44B-E	U12E U36C,E,F		U39A, D,E						

NECTIONS.
D SPARE



	14520	74161	75150	75152	TR1602A	MC4024P
	U17	U1	U3	U4	U10	U19
	8	8	A	8	D	A
	16	16	(+12V) 13	(+12V) 16	1	14
	8	8	3	8	3	7
			(-12V) 10		(-12V) 2	

Figure 5. Type 791201 Asynchronous I/O, Schematic Diagram